IN THE SPECIFICATION

Please replace paragraph starting on page 9 line 16 with the following paragraph:

The n-type region 206 located between the source/drain extensions 242 defines the channel region 250 of device 200. As shown in Figure 2, the source/drain regions are formed with a recess etch which creates a source/drain extension geometry which concaves inward creating an inflection point 260. The inflection point 260 is the location where the source/drain regions extend the greatest lateral distance beneath of gate electrode 202. In this way, when the recesses are back filled with highly conductive silicon or silicon alloy the distance between the source/drain extension regions is larger directly beneath the gate dielectric than is the distance deeper into the n-type region. That is, in accordance with an embodiment of the present invention source/drain regions are formed in a manner which creates a channel region 252 directly beneath the gate dielectric with a larger physical or metallurgical channel length (L_{met}) **than** the channel region 254 deeper into the substrate between the inflection points 260. Such a unique geometry provides improved performance in both the "on" and "off" states of the device. When the device is "off", the channel region remains n-type (no inversion). In the off condition any leakage (I_{off}) is due to holes traveling from the source/drain extension region to the other source/drain extension region directly beneath the gate oxide in region 252. In the off condition, holes experience a large channel length which greatly reduces the leakage current (i.e., reduces I_{off}). On the other hand, when device 200 is in the "ON" condition, n-type region 206 forms a channel by inverting the n-type silicon into p-type silicon. The inversion region forms a channel deeper into the substrate than the depth at which the inflection point 260 occurs. In this way, when the device is in the "on" condition and the inverted channel formed, a smaller L_{met} is

A1

cont. realized. A smaller L_{met} during the "ON" state directly translates to a smaller channel resistance which results in a higher I_{on}.

A1

Please replace paragraph starting on page 13 last line with the following paragraph:

According to the present invention a thin spacer layer 308 is formed over substrate 300 including n-well 302 and the top and sides of gate electrode 306 as shown in Figure 4. Spacer layer 308 will subsequently be used to form sidewall spacers for the MOS device. Spacer layer 310 is formed to a thickness between 50-300Å. It is to be appreciated that spacer layer 308 must be formed thick enough to electrically isolate a subsequently deposited silicon or silicon alloy film from gate electrode 306.

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Please replace paragraphs starting on page 19 line 16with the following paragraph:

Next, as shown in Figure 8, a thin, approximately 50-100Å chemical vapor deposited (CVD) oxide layer 322 is blanket deposited over substrate 300 including silicon or silicon alloy film 318, sidewall spacers 310 and isolation regions 304. Oxide layer 322 can be formed by any well known CVD process. In a preferred embodiment however the deposition temperature is kept below 750°C in order to not activate or disturb the dopants in the silicon or silicon alloy. An oxide deposition temperature of approximately 650°C is preferred. Next, a substantially thicker, 500 to 1800Å with 800Å, CVD silicon nitride layer 324 is blanket deposited onto oxide layer 322. Silicon nitride layer 324 is preferably formed by a standard CVD "hot wall" process at a temperature below 750°C and a temperature of 750°C being ideal. By keeping the silicon nitride deposition temperature relatively low the thermal budget is kept down and the deposition rate and uniformity made more controllable. Oxide layer 322

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